CLEAN COPY OF CLAIMS AS AMENDED:

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(Amended) 3. Circuit configuration as defined in Claim 1, characterized in that a pole of the supply voltage source (U) is connected to an input of two-wire sensor (S) via a HART® resistor (RH), the drain source path of a field effect transistor (T1), and the current-limiting resistor (R1), the other input of which sensor is connected to the other pole of the supply voltage source (U) via the second connection line (V2) that the HART® resistor (RH), the drain source path of the field effect transistor (T1) and the current-limiting resistor (R1) are positioned in the first connection line (V1), that the source electrode of the field effect transistor (T1) is connected to the second connection line (V2) via a series circuit comprising a first and second limiting diode (D1, D2), that a first resistor (R4) is positioned parallel to the second limiting diode (D2), that the joint node of the second limiting diode (D2) and the first resistor (R4) is connected to the base of a transistor (T2), the collector of which is connected to the gate

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electrode of field effect transistor (T1) via a second resistor (R3), and the emitter of which is connected to the second connection line (V2), and that the gate electrode of the field effect transistor (T1) is connected to the source electrode via a third resistor (R2).

A2 (Amended) 5. Circuit configuration as defined in claim 4, characterized in that the series connected limiting diodes (D1 through D6) are oppositely poled.
